AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph on page 4, lines 2-11 with the following amended paragraph.

A mixer circuit in accordance with the invention includes a first mixer stage comprising a first transmission gate and a second transmission gate. The first transmission gate is coupled with a first ~~mixed~~ MIXED signal terminal and first and second local oscillator (LO) signal terminals. The second transmission gate is coupled with a second MIXED signal terminal and the first and second LO signal terminals. The mixer further includes a second mixer stage comprising a third transmission gate and a fourth transmission gate. The third transmission gate is coupled with the first MIXED signal terminal and the first and second local oscillator signal terminals so as to operate out of phase with the first transmission gate. The fourth transmission gate is coupled with the second MIXED signal terminal and the first and second local oscillator signal terminals so as to operate out of phase with the second transmission gate.

Please replace the paragraph on page 6, line 12 through page 7, line 2 with the following amended paragraph.

Referring now to Figure 1, a schematic diagram of a prior art complementary-metal-oxide semiconductor (CMOS) passive mixer circuit 100 is shown. The mixer 100 comprises a first stage 105 and a second stage 110. Each stage comprises two n-type field effect transistors (FETs). In this regard, the first mixer stage 105 comprises FETs 115 and 120. The second stage 110 comprises FETs 125 and 130. The mixer 100 also comprises radio frequency (RF) mixed signal terminals 135 and 140 and local oscillator (LO) signal terminals 145 and 150. The RF mixed signal terminals 135 and 140 are used to communicate RF mixed signals to and/or from

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the mixer 100, such as for use in a radio receiver, transmitter and/or transceiver. The LO signal terminals 145 and 150 are used to supply a LO signal to the mixer 100 for use in up-converting and/or down-converting signals processed by the mixer 100. The mixer 100 further comprises base band signal terminals 155 and 160, which are used to communicate base band signals (e.g. voice) to and/or from the mixer 100. As was noted above, while this disclosure is generally directed to RF applications, it will be appreciated that other applications for such mixer circuits exist.

Please replace the paragraph on page 9, lines 1-10 with the following amended paragraph.

The mixer 200 comprises a first mixer stage 205 and a second mixer stage 210. The first mixer stage 205 comprises a first transmission gate 215 and a second transmission gate 220. The second mixer stage comprises a third transmission gate 225 and a fourth transmission gate 230. For the mixer 200 the first transmission gate 215 is coupled with the third transmission gate 225 in a first "circuit path" and the second transmission gate 220 is coupled with the fourth transmission gate 230 in a second "circuit path." In this respect, such a configuration may address at least some of the disadvantages of the mixer 100 shown in Figure 1 and described above ~~by~~. Such improvements result, at least in part, from an increase in the linear range of such a mixer circuit due to the use of the transmission gates 215-230. These improvements will be discussed further with respect to Figures 3 and 4.

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Please replace the paragraph on page 10, lines 5-13 with the following amended paragraph.

Referring now to Figure 3, a schematic diagram of a mixer circuit 300 according to another embodiment of the invention is shown. It is noted that the mixer circuit 300 contains analogous elements to the mixer circuit 200 shown in Figure 2. In this regard, elements of the mixer 300 that are analogous to those of the mixer 200 have been referenced with corresponding 300 series reference numerals. For example, while the first ~~transmission gate~~ stage of the mixer 200 is referenced as 205, ~~the~~ a first ~~transmission gate~~ stage of the mixer 300 is referenced as 305. This convention is consistent throughout Figure 3. For the sake of brevity, these analogous elements will only be described, with respect to Figure 3, to describe the function of the mixer 300 with respect to the additional detail of the transmission gates ~~305~~315, ~~310~~320, ~~315~~ 325 and ~~320~~330.

Please replace the paragraph on page 10, lines 14-23 with the following amended paragraph.

In this regard, the transmission gates ~~305~~315, ~~310~~320, ~~315~~ 325 and ~~320~~ 330 of the mixer 300 comprise CMOS transmission gates, each having an n-type field-effect transistor (FET), respectively 317, 322, 327 and 332; and a p-type FET, respectively 319, 324, 329 and 334. Each n-type FET has a source terminal and a drain terminal coupled, respectively, with a source terminal and a drain terminal of its corresponding p-type FET. Further, the source terminals of the n-type FETs 317 and 327 and the p-type FETs 319 and 329 of the first transmission gate 315 and the third transmission gate 325 are coupled with the first mixed signal terminal 335. Likewise, the source terminals of the n-type FETs 322 and 332 and p-type FETs 324 and 334 of

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the second transmission gate 320 and the fourth transmission gate 330 are coupled with the second mixed signal terminal 340.

Please replace the paragraph on page 12, lines 9-19 with the following amended paragraph.

Also, the mixer 300 may be implemented on an integrated circuit, such that the first, second, third and fourth transmission gates (315, 320, 325 and 330) are substantially physically symmetric. Further, the first and second transmission gates (315 and 320) may be implemented so as to have the same orientation with respect to each other, while the third and fourth transmission gates (325 and 330) also have the same orientation with respect to each other. Such an arrangement may provide additional advantages over other techniques, such as those using discrete components. In this regard, such a configuration would reduce the amount of LO signal feedthrough. Such LO signal feedthrough results, at least in part, from mismatch (e.g. differences in electrical characteristics) in the transistors used to implement such a mixer circuit. Therefore, because such transistors will be closely matched, implementing the mixer 300 in the above-described fashion will reduce mismatches over other possible techniques.

Please replace the Abstract on page 24, lines 2-11 with the following amended Abstract.

A mixer circuit in accordance with an embodiment of the invention includes a first mixer stage ~~comprising~~ including ~~a~~ first and second transmission gates, and a second mixer stage ~~comprising~~ including third and fourth transmission gates. The mixer further includes a first base band signal terminal coupled with the first and second transmission gates and a second base band signal terminal coupled with the third and fourth transmission gates. The mixer circuit processes

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signals so as to mix a base band signal communicated to the first and second base band signal terminals with a differential LO signal communicated to first and second LO signal terminals to create a first mixed differential signal. Alternatively, the mixer extracts a base band signal from a mixed signal communicated to the first and second mixed signal terminals signal using the LO signal communicated to the first and second LO signal terminals.

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